

EAST - [default.wsp:1]

File View Edit Tools Window Help

Drafts
Pending
Active

- L1: (21) memory and ((data adj buffer) same ((delay adj l
- L2: (4) "6438060"
- L3: (4) 2 and characteristic
- L4: (2) 3 and dc
- L5: (11) 1 and characteristic
- L6: (0) 5 and (dc adj signal)
- L7: (0) 5 and (dc near3 signal)

DBs: USPAT;US-PGPUB;EPO;JPO

Default operator: OR

P: Highlight all hit terms initially

	Type	L #	Hits	Search Text	DBs
1	BRS	L1	21	memory and ((data adj buffer) same ((delay adj lock adj loop) or dll) same clock)	USPAT; US-PGPUB; 20 EPO; JPO
2	BRS	L2	4	"6438060"	USPAT; US-PGPUB; 20 EPO; JPO
3	BRS	L3	4	2 and characteristic	USPAT; US-PGPUB; 20 EPO; JPO
4	BRS	L4	2	3 and dc	USPAT; US-PGPUB; 20 EPO; JPO
5	BRS	L5	11	1 and characteristic	USPAT; US-PGPUB; 20 EPO; JPO
6	BRS	L6	0	5 and (dc adj signal)	USPAT; US-PGPUB; 20 EPO; JPO
7	BRS	L7	0	5 and (dc near3 signal)	USPAT; US-PGPUB; 20 EPO; JPO
8	BRS	L8	3	5 and dc and signal	USPAT; US-PGPUB; 20 EPO; JPO

Ready

NUM

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Active

- L1: (21) memory and ((data adj buffer) same ((delay adj 1
- L2: (4) "6438060"
- L3: (4) 2 and characteristic
- L4: (2) 3 and dc
- L6: (0) 5 and (dc adj signal)
- L7: (0) 5 and (dc near3 signal)
- L8: (3) 5 and dc and signal
- L5: (11) 1 and characteristic

Failed

Saved

Favorites

Tagged (2)

UDC

DBv: USPAT:US:PGPUB:EPO:JPO

Default operator: OR

1 and characteristic

Current OR Current XR

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XR
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20040044933 A1	20040304	14	Memory technology test apparatus	714/718	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20030001621 A1	20030102	10	Data I/O circuit of semiconductor memory device	326/93	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20020181639 A1	20021205	9	Adaptive de-skew clock generation	375/373	375/354; 375/376
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020027451 A1	20020307	34	SEMICONDUCTOR DEVICE	326/105	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6530006 B1	20030304	11	System and method for providing reliable transmission in a buffered memory system	711/167	710/52; 711/105
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6480033 B2	20021112	32	Semiconductor device	326/105	326/93; 365/230 06;
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6376869 B1	20020423	16	Semiconductor device	257/288	257/296; 257/298;
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6269051 B1	20010731	46	Semiconductor device and timing control circuit	365/233	331/51; 365/194
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6212127 B1	20010403	48	Semiconductor device and timing control circuit	365/233	365/194
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6084802 A	20000704	24	Semiconductor integrated circuit device	365/189.05	365/233
11	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5990730 A	19991123	24	Semiconductor device with stable operation and reduced power consumption	327/544	327/143; 365/227

Ready

NUM